

Late Tuesday Afternoon

POSTER SESSION

Tuesday, May 22 / 4:00 – 7:00 pm / Exhibit Hall A

ACTIVE-MATRIX DEVICES

P.1: WITHDRAWN

P.2: Photosensitive Organic Passivation TFTs with High Anti-Water-Absorption Ability

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A photosensitive organic passivation for conventional back-channel-etched (BCE) thin-film transistors (TFTs) has been investigated, resulting in a reduction in the number fabrication process steps and an increased aperture ratio. These devices also exhibit lower leakage current than conventional silicon nitride (SiN_x) passivation-layer BCE TFTs. The leakage currents between indium tin oxide (ITO) pixels and the TFT devices, as well as the thermal-humidity reliability tests have also been investigated.

P.3: Laser-Assisted ITO Lift-Off for TFT Fabrication

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For the first time, an excimer laser was used to fabricate a back-channel-etched (BCE) a-Si TFT. A KrF laser easily and successfully lifts-off ITO on photoresist, saving much process time from eliminating a mask alignment step. The mechanism of laser-assisted ITO lift-off (LAIL) technology was carefully studied. TFT devices fabricated by LAIL technology exhibits the same electrical performance as traditional non-lift-off devices.

P.4: Metal-Contact Improvement in Cu-Gate TFT-LCDs

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It was found that copper was damaged in via-hole etching using SF_6 and O_2 plasma. From TEM and XPS analysis, an etching by-product composed principally of Cu_2O was formed on the Cu film after via etching. The via contact resistance between Cu and ITO could be improved to be the same as the conventional Al gate metal by optimizing the ratio of SF_6 and O_2 .

P.5: Solution-Processed SiO_2 Films Using Hydrogenated Polysilane-Based Liquid Materials

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Polycrystalline-silicon thin-film transistors (poly-Si TFTs) have been fabricated using solution-processed SiO_2 films made from a polysilane-based liquid precursor. By using this precursor, gate silicon oxide films were prepared by spin-coating, from which TFTs with mobilities of $108.9 \text{ cm}^2/\text{V}\cdot\text{sec}$ were fabricated and the gate leakage current was sufficiently low.

P.6: Top- and Bottom-Gate Amorphous ZnO Transparent TFTs Fabricated by All-Etching Processes

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Both top- and bottom-gate amorphous ZnO TFTs were effectively fabricated by thinning the ZnO layer and by using all-etching processes. Rather high field-effect mobilities of 25 and 4 cm²/V-sec and on/off current ratios of >10⁻⁷ and >10⁻⁶ were achieved for top- and bottom-gate configurations, respectively.

P.7: An a-Si TFT-LCD with an Embedded Color Image Scanner

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A 4-in. (qVGA, 320 × 240, 262,144 colors) a-Si thin-film-transistor liquid-crystal display (TFT-LCD) with an embedded color image scanner was developed. The sensing and display devices were simultaneously fabricated by conventional a-Si processes, resulting in a thinner panel with improved scanning image quality.

P.8: a-Si:H TFT-LCDs with a Single Organic Passivation Layer

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A 1.9-in. qCIF TFT-LCD with novel photosensitive organic material as the single passivation layer was successfully fabricated. The leakage current of the a-Si:H TFTs with a single organic passivation layer is lower than the one with SiN_x layers and the adhesion strength is sufficiently strong so that the overlap between the ITO pixel electrode and the data lines can be formed.

P.9: Unified Model and Prediction Technique for On-Current Degradation Caused by Drain-Avalanche Hot Carriers in LTPS TFTs

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A unified model and a prediction technique for on-current degradation in NMOS low-temperature polysilicon thin-film transistors (LTPS TFTs) will be presented. The increase in resistance is expressed as a function of stress-drain current and stress-drain voltage. By using this technique, the turnaround time for circuit design can be shortened.

P.10: Transparent OTFTs with Color-Filtering Functional Gate Insulators

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Transparent organic thin-film transistors (OTFTs) impregnated with nanoparticles, organic dyes, and pigments into the dielectric insulators were fabricated and analyzed. The colored composite insulators were utilized as the color filter and the diffusion layer simultaneously to obtain the desired color and to minimize glare. OTFTs with the above-mentioned composite dielectric layers possess color filtering and anti-glare functions comparable to those of conventional devices, while significantly reducing OTFT light sensitivity.

P.11: Analysis of Low-Power-Consumption AMOLED Displays on Flexible Stainless-Steel Substrates

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Simulations and results that demonstrate the viability of metal foil as a substrate for low-power-consumption flexible AMOLED displays will be presented. By using organic planarization layers, very smooth surface properties can be achieved, thus resulting in excellent TFT performance and capacitive coupling effects that only have a minimal impact on power consumption and a small impact on gate-line delays. By using phosphorescent OLEDs, the power consumption of 40-in. AMOLED displays were analyzed.

P.12: Enhanced Pentacene OTFTs with Suspended Source/ Drain Electrode

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Tri-isopropylsilyl pentacene organic thin-film transistors (OTFTs) with suspended source/drain electrodes that improved the electrical properties were fabricated. The suspended electrodes were fabricated using a sacrificial Cr/Au double layer. By completely etching the Cr layer in the active area, a suspended Au source/drain structure was constructed with a top-contact-like geometry. The field-effect mobility of these ink-jet-printed TIPS pentacene OTFTs increased from 0.007 to 0.066 cm²/V-sec, the on/off ratio increased from 104 to 106, V_{th} decreased from +9 to -3 V, and the subthreshold slope decreased from 4.5 to 0.9 V/decade.

P.13: Low-Power a-Si Level Shifter for Mobile Displays with Bootstrapped Capacitor and Pulsed Signal Source

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A low-power-consumption a-Si level shifter was designed and verified by SPICE simulation. The level shifter of cascaded inverters shifts low voltage (5 V) to high voltage (23 V) by employing a bootstrapping method. Simulations indicate that the level shifter reduced the power consumption by 50% to 4 mW.

P.14: a-Si Robust Gate Driver for 7.0-in. WVGA LCD Panel

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An a-Si robust gate driver on glass substrate for 7-in. WVGA-format panels was developed. The gate driver compensates the threshold-voltage (V_{th}) shift from electrical stress and operates correctly despite unstable V_{th} voltages. The driver was integrated on 7-in. WVGA a-Si:H TFT panels

P.15: AMOLED Pixel Structures Compensating the Hysteresis of Poly-Si TFTs

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A new voltage-programmed AMOLED pixel circuit is proposed. The measurement data indicates that the new pixel is less sensitive to the hysteresis of LTPS TFTs than the conventional 2T1C pixel structure and can improve the recoverable residual image due to the hysteresis characteristics of LTPS TFTs.

P.16: Solution-Processed Zinc Oxide TFTs

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Methods for producing zinc oxide thin-film transistors by solution processing were studied. One class of methods involves the use of zinc-acetate-based precursor solutions, while the other involves the use of preformed nanoparticles. Devices with reasonable transfer characteristics were obtained from both routes, exhibiting mobilities typically greater than $0.1 \text{ cm}^2/\text{V}\cdot\text{sec}$.

P.17: Metal-Induced Continuous-Zonal-Domain Poly-Si TFTs

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Metal-induced polycrystalline-silicon (poly-Si) films with continuous zonal domain (CZD) were fabricated by pre-defining crystalline nuclei lines on a nano-layer of silicon dioxide. The impact of glass substrate shrinking on subsequent alignment processing has been taken into account. The crystallization process is controllable and the annealing time is shorter than 1 hour. The P-channel thin-film transistors (TFTs) exhibit high performance and uniformity.

P.18: Improvement of Stability in ZnO TFTs under Bias Stress

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The stability of ZnO TFT under bias stress was investigated. Transparent ZnO thin films deposited by means of atomic layer deposition (ALD) at 100°C and plasma-enhanced atomic layer deposition (PEALD) at 150°C were used as the active channel. The TFT with a PEALD-grown ZnO layer has better stability under bias stress than the TFT with an ALD-grown ZnO layer.

P.19: Investigation of Deposition-Rate Effects on the Current–Voltage Characteristics of Organic Dynamic-Random-Access Bistable Devices

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Organic dynamic-random-access devices with an Al/Alq₃/n-doped Si structure at different deposition rates were investigated. This device contains a heterostructure and only two-layer deposition is required. Current–voltage characteristics are similar to that of a metal/organic semiconductor/metal structure, and this three-layer structure is useful in organic memory devices. This device involves an extremely simple fabrication process and shows great potential for fabricating flexible organic displays.

P.20: Highly Integrated 10.2-in. WVGA LTPS-LCD Manufactured by PMOS Process

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A highly integrated 10.2-in. WVGA LTPS LCD with a single-chip ASIC manufactured by a PMOS process was developed. Level shifters, dc-dc converters for V_{DD} and V_{EE} , two-phase shift registers with forward/reverse scanning, and a 1:6 demultiplexer were integrated on glass. The ASIC includes a timing controller and a 400-channel source driver. This architecture dramatically reduces cost and provides high mechanical robustness. The six-mask PMOS process also improves the throughput and reduces manufacturing yield loss.

P.21: Jet-Printed All-Additive Active-Matrix Pixel Circuits on Low-Temperature Flexible Substrates

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Flexible active-matrix pixel circuits were fabricated in an all-additive method using solution processes and ink-jet printing. The maximum process temperature was below 200°C. The prototype pixel circuits with 50 × 50 pixels (680- μ m pixel pitch) are based on PQT-12 organic semiconductor, a PVP gate dielectric, and silver nanoparticle conductors. The measured TFT and pixel performance is promising for paper-like displays.

P.22: Single-Grain Si TFTs and Circuits for Flexible Electronics and 3-D ICs

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TFTs were fabricated inside location-controlled Si grains through the Czochralski process using an excimer laser. Single-grain TFTs and inverters fabricated at 350°C showed a mobility of 597 cm²/V-sec and a propagation delay of 3.1 nsec. By combining a-Si by sputtering and SiO₂ by ICPECVD, SG-TFTs were fabricated with a maximum temperature of 100°C. A mobility of 289 cm²/V-sec was successfully obtained.

P.23: Design Parameters for Using Charging Technique for TFT-LCDs

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A well-known pre-charging technique based on charging a pixel two times at an interval of one gate pulse width was used. However, there is a side effect of a pattern being out of focus. To remove this side effect, a charging design parameter was optimized. A120-Hz 32-in. WXGA TFT-LCD, having three times the $C_{st} + C_{lc}$ as that for a conventional IPS structure, was developed.

P.24: Design of Low-Cost 2.2-in. qVGA LTPS TFT-LCD Panel

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A 2.2-in. qVGA LTPS TFT-LCD panel driven by external output buffers to reduce the display system cost is proposed. The proposed panel adopts a 1:6 de-multiplexing scheme that decreases the height of the source driver to 40% compared with that of a conventional structure for a 1:3 de-multiplexing scheme.

P.25: Power-Consumption Characteristics and Simulation of LCD Panels

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A detailed investigation showed that the digital part, analog circuit, column driver, and row driver determine the power consumption of an LCD. The power-consumption characteristics of a WXGA-resolution LCD were determined, and thus suggest how to simulate the power consumption in an arbitrary pattern. This simulation method could improve the design of a large-sized high-resolution panel to lower the power consumption.

P.26: WITHDRAWN

P.27: Anomalous Increased Drain-Current Characteristics of a-Si:H TFTs with Long Channel Width

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Channel-width-split a-Si:H TFTs ranging from 40 to 48,000 μm were fabricated on glass substrates to investigate the channel-width dependency of the electrical characteristics. TFTs with a channel width larger than 10,000 μm show that the width-normalized drain current increases significantly as a result of an increased field-effect mobility due to the dissipated power at the drain edge and n-p-n bipolar action.

P.28: Flexibility Study of High-Performance LTPS TFTs on Flexible Metal Foil

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The flexibility of p-channel LTPS TFTs on 150- μm metal foil was studied. The non-laser poly-Si TFTs exhibited a field-effect mobility of 108 $\text{cm}^2/\text{V}\cdot\text{sec}$, a threshold voltage of -6.7 V and a gate voltage swing of 0.9 V/dec., and a minimum off current of 10–12 $\text{pA}/\mu\text{m}$ at $V_{\text{ds}} = -0.1$ V. The TFT performance is stable up to 10,000 bending cycles with a strain of 0.6%.

P.194L: Late-News Poster: High-Frequency Performance of Sub-Micrometer Channel-Length Si TFTs Fabricated on Large-Grain Poly-Si Films

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High-frequency characteristics of submicron Si TFTs fabricated on large-grain poly-Si films were demonstrated for the first time. A cutoff frequency f_{T} of 6 GHz and a maximum oscillation frequency (f_{max}) of 25 GHz were obtained for the TFT with a channel length of 0.5 μm . It was confirmed that the use of insulating substrates is advantageous in reducing the parasitic susceptance due to the use of a conductive substrate, thereby increasing f_{max} .

P.195L: Late-News Poster: A High-Resolution LTPS AMLCD with Integrated 8-bit DAC

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A 222-dpi LTPS AMLCD with an integrated 8-bit DAC for reduced system cost will be described. The architecture is based on a two-stage resistor–capacitor DAC with a two-way interleaved architecture that is well suited to high-resolution LTPS displays. High-uniformity images on a 1.8-in. QVGA display were confirmed.

P.196L: Late-News Poster: High-Performance Zinc Oxide Transistors by an Ambient Process

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An ambient process was developed for both the dielectric and semiconductor layers of a zinc-oxide-based thin-film transistor. The dielectric films exhibited good electrical properties, leading to devices with a gate leakage less than 25 nA/cm^2 . Typical devices had mobilities in excess of 5 $\text{cm}^2/\text{V}\cdot\text{sec}$ for a maximum substrate temperature of 200°C. In addition, these novel devices showed reasonable electrical stability.

P.197L: Late-News Poster: Demonstration of High Performance TFTs on Silicon-on-Glass (SiOG) Substrate

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A new low-temperature crystalline silicon (LTCS) substrate and device technology will be reported. The fabrication and analysis of CMOS devices fabricated using LTCS will be presented. The LTCS devices are comparable to those fabricated on SOI wafers with respect to carrier mobility and off-state leakage current, clearly demonstrating the potential for system-on-panel integration.

P.198L: Late-News Poster: Integrated Ambient-Light Sensors in LTPS AMLCDs

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Sensing ambient light in mobile applications allows for reduced power consumption through backlight control. The integration of light sensors reduces the module complexity, and placing the sensors close to the pixel array simplifies integration into products. An integrated ambient-light sensor consisting of lateral pin diodes and a digital read-out circuit will be described.

P.199L: Late-News Poster: Silicon Nanocrystal Photo-Sensor Integrated on LTPS Panels

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A photodetector having a silicon nanocrystal layer sandwiched in between two electrodes is proposed and was demonstrated for photosensing applications on LTPS panels for the first time. Through post-annealing of the silicon-rich oxide films, Si nanocrystals were formed with good uniformity and high-temperature tolerance to respond best to certain absorption spectrum of the corresponding light source. These silicon nanocrystals, less than 10 nm in diameter, exhibit a better quantum-confinement effect, thus promoting electron-hole-pair generation in the photosensing region as a result of its direct band gap.